When do we need Non-Quasistatic CMOS RF-Models?

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Abstract

This paper presents criteria for the onset of NQS effects derived from time transient device simulations and S-parameter measurements. For the first time it has been proved that e.g. a 10 μm NMOS transistor can be described up to 27 MHz and a 0.2 μm device up to 46 GHz by the quasistatic approach while the accuracy of the description of the inversion layer charge is still 99 %.

Introduction

Due to continuous down-scaling CMOS-technologies are playing a more important role in RF systems. Therefore there is a strong demand for compact small signal models describing accurately also the high-frequency region. An often mentioned problem hereby seem to be non-quasistatic phenomena. In contrast to (1, 2, 3) this paper will show, however, that their influence is often over-estimated under small signal conditions.

The aim of this paper is to determine the transition between quasistatic and non-quasistatic effects in terms of the frequency, the channel length and the applied voltages. Thus, it will be possible to estimate a theoretical limit up to which quasistatic MOSFET models are reasonable.

Fig. 1 summarizes our proceeding in a flowchart.

Quasistatic Operation Assumption

The device behaves quasistatically as long as the terminal voltages are varied slowly enough for the charge to follow "immediately" at any position in the device. Then, these charges can be assumed identical to those that would be found if DC voltages were used instead (4). This can be interpreted in the way that the NQS operation starts as soon as the inertia of the charge carriers can not be neglected any more.

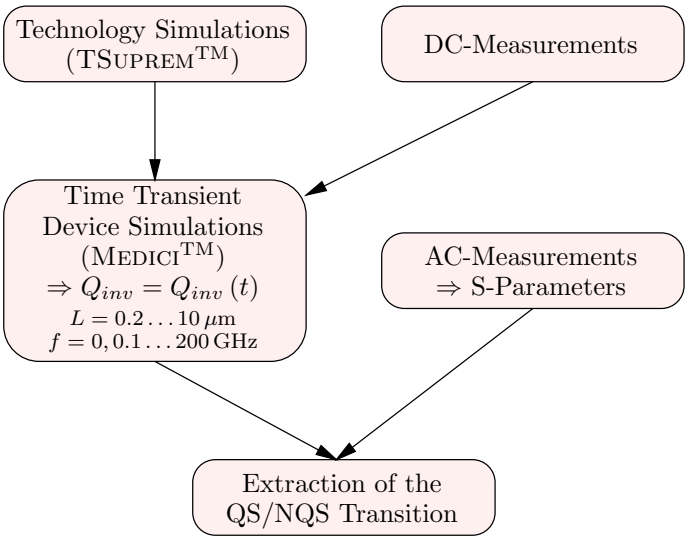

Fig. 1: Proceeding of our investigations.

According to AC considerations our work focuses on the small variation of the inversion layer charge $\Delta Q_{inv}(t)$ (fig. 2). This contrasts to the normal approaches which investigate the turn-on and turn-off behavior since the large-signal channel build-up lasts much longer than its reaction on small signal variations.

Device Simulations

As the transient behavior of the channel inversion layer charge $Q_{inv}(t)$ can not be measured, we have performed extensive device simulations (Medici™) in time transient mode. In order to stay as close as possible to our measured device performance, we executed technology simulations (TSuprem™) on a commercial quarter-micron process as input for our device simulations.

As RF devices are mainly used for analog circuits, saturation is surely the most important operation region. There-

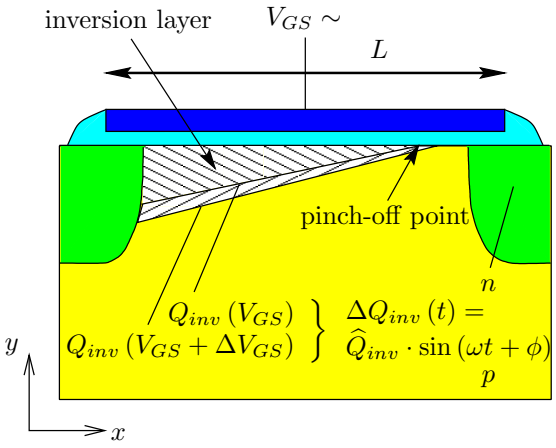

Fig. 2: Scheme of inversion layer along the channel at different gate biases.

fore the following investigations will focus on a typical AC operation point of

$$V_{GS} = 1.5\,\mathrm{V} \approx (V_{CC} - V_{th})/2 \quad \text{and} \quad V_{DS} = 2.5\,\mathrm{V}.$$

If we apply $V_{GS}(t) = 1.5\,\mathrm{V} + 0.01\,\mathrm{V}\cdot\sin(\omega t)$ as time transient AC gate voltage, we expect the total inversion charge

$$Q_{inv}(t) = \int_0^L Q'_{inv}(t)\,\mathrm{dx} = Q_{inv,DC} + \widehat{Q}_{inv}\cdot\sin(\omega t+\phi)$$

to vary sinusoidally between its DC extremes of $Q_{inv}(1.5\,\mathrm{V}\pm 0.01\,\mathrm{V}) = \pm\widehat{Q}_{inv}(f\to 0)$.

Fig. 3 shows the frequency-normalized transient response of the inversion charge $Q_{inv}(t)$ to the applied gate bias.

The amplitude $\widehat{Q}_{inv}$ of the inversion layer charge decreases with higher frequencies, and its phase shift ϕ increases. Note, that the channel charge of a $0.25\,\mu$m MOSFET varies only by about 60 carriers per μm width for a gate voltage variation of 10 mV. Therefore very exact simulations were required.

To achieve a smooth sine wave and to include the nonlinearities of the devices, 256 time steps were needed for each frequency and gate length simulation.

The characteristic values ($\widehat{Q}_{inv}$, ϕ) depending on the frequency f and the gate length L can be seen in the following figures: the amplitude $\widehat{Q}_{inv}$ of the inversion layer charge (fig. 4) remains nearly constant up to a certain frequency limit and then decreases steeply, whereas the phase shift ϕ (fig. 5) varies linearly with the frequency.

From these figures we can extract a frequency limit f_{NQS} (figs. 6 and 7) that guarantees the desired accuracy.

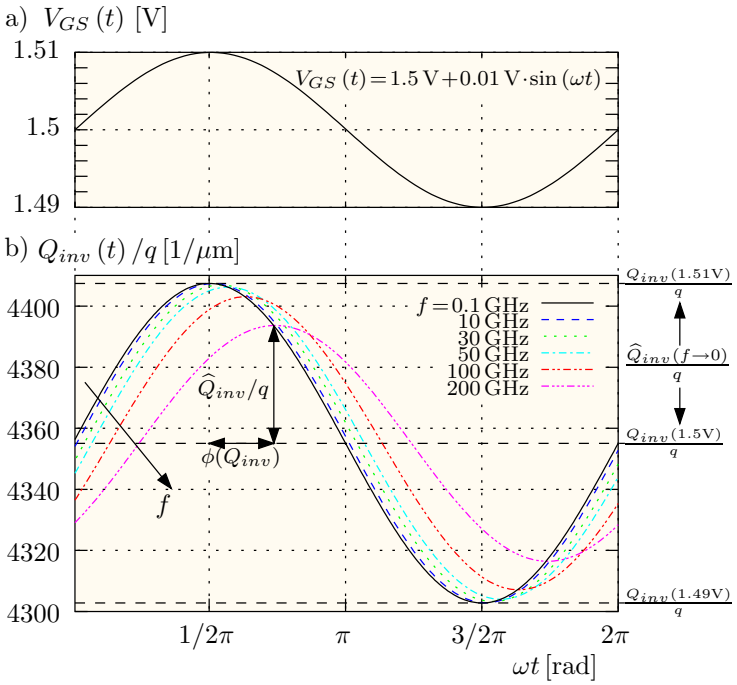

Fig. 3: a) Applied gate voltage vs. time ($V_{DS} = 2.5\,\mathrm{V}$) for transient analysis with 256 time steps/period b) Inversion layer charge of a MOSFET with $L = 0.25\,\mu$m ($W = 1\,\mu$m) varying in amplitude and phase according to the applied gate bias for different frequencies.

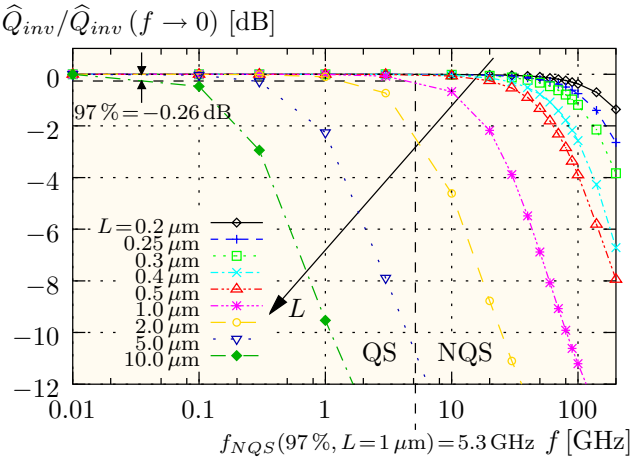

Fig. 4: Normalized inversion layer charge amplitude vs. applied frequency ($V_{GS} = 1.5\,\mathrm{V}$, $V_{DS} = 2.5\,\mathrm{V}$, $W = 1\,\mu$m) in logarithmic scale for different gate lengths.

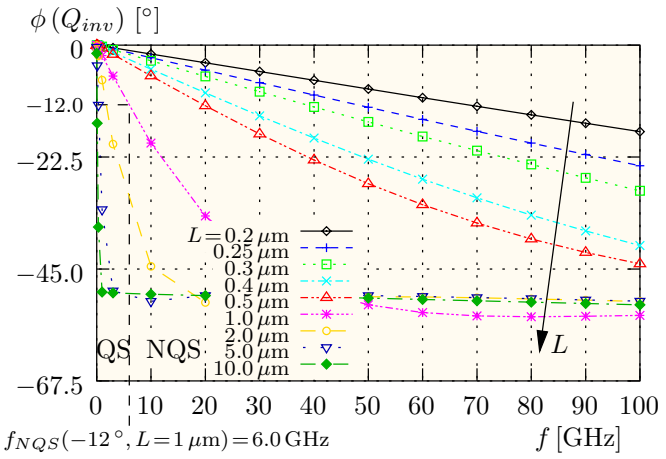

Fig. 5: Phase of the inversion layer charge vs. the applied frequency for different gate lengths.

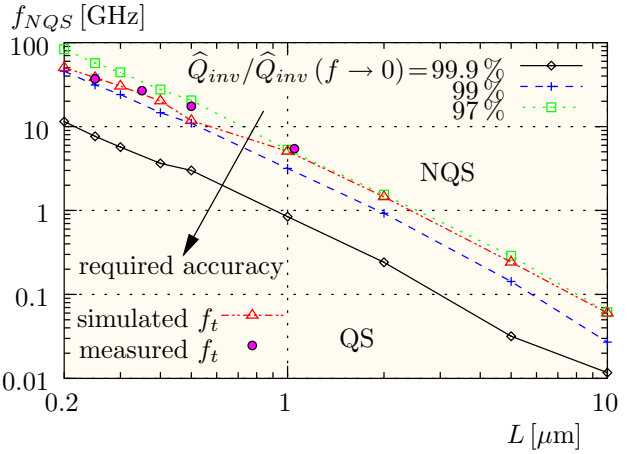

Fig. 6: Frequency limit f_{NQS} derived from the decrease of the charge amplitude vs. gate length in comparison with f_t.

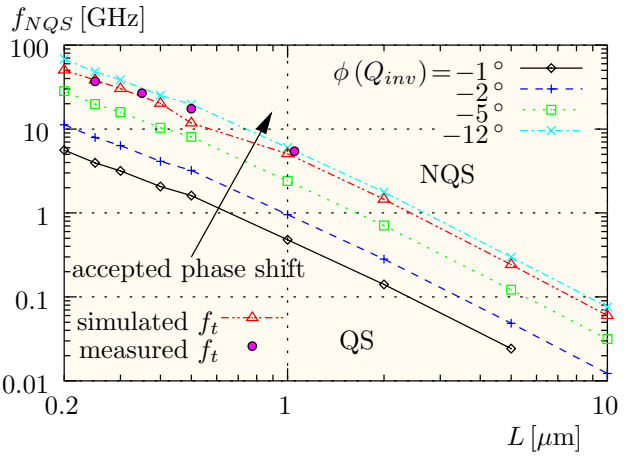

Fig. 7: Frequency limit f_{NQS} derived from the phase shift of the charge vs. gate length in comparison with f_t.

We define the accuracy as the deviation of the magnitude and phase of the inversion charge from their DC values $\widehat{Q}_{inv} = \widehat{Q}_{inv}\,(f \to 0) = Q_{inv}\,(1.51\text{V}) - Q_{inv}\,(1.50\text{V})$ and $\phi\,(Q_{inv}) = 0$.
Up to this frequency f_{NQS} no effects on the small signal parameters can be observed for a given gate length.

The advantage of our strategy is a physics-based well-defined separation of the inner transistor from parasitic effects (5, 6).

Measurements and Discussion

To verify our observations RF measurements on CMOS finger structures ($W = 96\,\mu$m) in quarter micron technology were performed. The small-signal scattering parameters (S_{ij}) have been corrected using a two-step de-embedding technique with open and short structures (7).

In order to obtain a better relationship between our transient simulations and S-parameter measurements, the terminal currents have to be evaluated: the extracted unity current gain frequencies $f_t = f(\widehat{I}_D/\widehat{I}_G \equiv 1)$ of different devices show good agreement between our measurements and simulations (fig. 8).

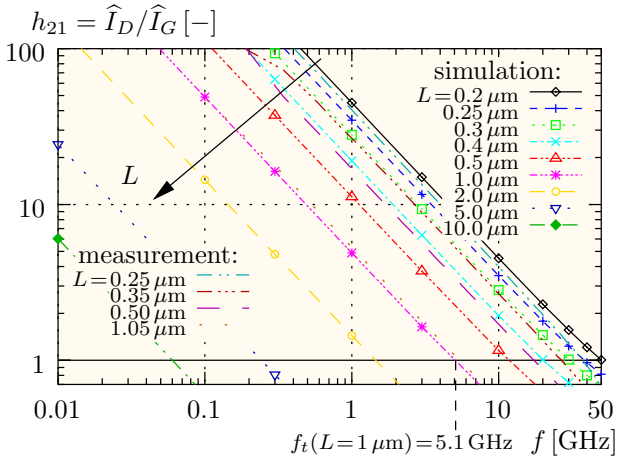

Fig. 8: Extraction of $f_t\,(L)$ from the unity current gain (measurement and simulation).

The measured phase shift ϑ of the current gain $h_{21} = \widehat{I}_D/\widehat{I}_G$ at f_t remains constant over a wide range of operating points in the saturation region (fig. 9), proving that our focus on simulating one typical operating point was justified.

Taking into account that circuits can not be operated above f_t, we were interested, which $\widehat{Q}_{inv}$ and ϕ devia-

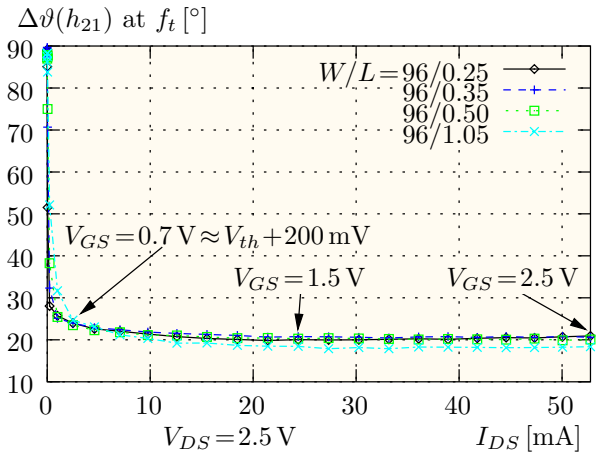

Fig. 9: Measured phase shift of the current gain $h_{21} = \widehat{I}_D/\widehat{I}_G$ at f_t vs. operating points for different gate length.

tions (figs. 6 and 7) have to be accepted for a desired frequency range: fig. 10 quantifies the deviation from the quasistatic assumption $\widehat{Q}_{inv}/\widehat{Q}_{inv}\,(f \to 0) = 1$ and $\phi\,(Q_{inv}) = 0$, and thus shows, up to which frequencies one can simulate quasistatically all gate lengths of the analysed technology.

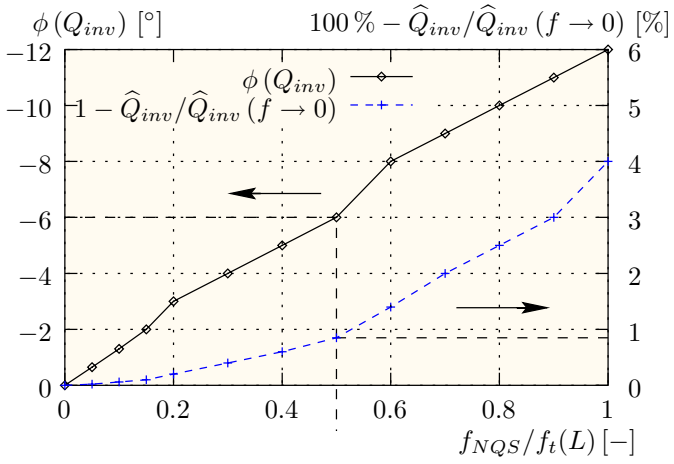

Fig. 10: Trade-off between decreasing accuracy and increasing frequency: e.g. for simulating quasistatically transistors with arbitrary gate length up to $1/2\,f_t$ a phase shift of $-6\,°$ and an amplitude accuracy of 99 % have to be accepted.

Conclusion

This paper presents criteria for the beginning of NQS effects. They depend on the applied frequency, the gate length, and especially the required accuracy, whereas the operation voltages turned out to be of minor importance. Various devices of a commercial process with gate lengths ranging from 0.2 to 10 μm have been investigated by time transient device simulations and S-parameter measurements.

It has been proved that e.g. with an accuracy of 99 % in the description of the inversion layer charge a 10 μm NMOS transistor can be described up to 27 MHz and a 0.2 μm device up to 46 GHz by the quasistatic approach. If we tolerate an accuracy in the amplitude of 96 % and in the phase shift of $-12\,°$, one is able to describe the MOSFETs' small signal behavior quasistatically up to $f_t\,(L)$ for all gate lengths. Otherwise a NQS approach is required. To our knowledge this is the first time that such numbers are reported.

References

(1) E. Abou-Allam and T. Manku. A small-signal MOSFET model for radiofrequency IC applications. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 16(5):437–447, May 1997.

(2) X. Jin, J.-J. Ou, C.-H. Chen, W. Liu, M. J. Deen, P. R. Gray, and C. Hu. An effective gate resistance model for CMOS RF and noise modeling. In *IEEE International Electron Devices Meeting Technical Digest (IEDM)*, pages 961–964, 1998.

(3) M. Bagheri and Y. Tsividis. A small signal dc-to-high-frequency nonquasistatic model for the four-terminal MOSFET valid in all regions of operation. *IEEE Transactions on Electron Devices*, 32(11):2383–2391, November 1985.

(4) Y. Tsividis. *Operation and Modeling of the MOS Transistor*. Electronics and Electronic Circuits. WCB McGraw-Hill, NewYork, 2. edition, 1999.

(5) E. Gondro, F. Schuler, and P. Klein. A physics based resistance model of the overlap regions in LDD-MOSFETs. In K. De Meyer and S. Biesemans, editors, *Simulation of Semiconductor Processes and Devices (SISPAD'98)*, pages 267–270, Leuven, Belgien, September 1998. Springer-Verlag Wien NewYork.

(6) E. Gondro, P. Klein, and F. Schuler. An analytical source-and-drain series resistance model of quarter micron MOSFETs and its influence on circuit simulation. In *IEEE International Symposium on Circuits and Systems (ISCAS'99)*, volume 6, pages 206–209, Orlando, Florida, USA, May/June 1999.

(7) M.C.A.M. Koolen, J.A.M. Geelen, and M.P.J.G. Versleijen. An improved de-embedding technique for on-wafer high-frequency characterization. In *IEEE Bipolar Circuits and Technology Meeting (BCTM'91)*, pages 188–191, 1991.