A Non-Linear Description of the Bias Dependent Parasitic Resistances of Quarter Micron MOSFETs

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***Abstract*–A new model description for source and drain resistances of LDD devices is proposed. It includes the dependence on the gate, bulk and drain bias.**
Measurements on a 0.25 μm gate length device show excellent agreement with circuit simulation.

1. Introduction

Scaling of MOSFETs requires more and more accuracy in the description of the parasitic resistances R_S and R_D of the source and drain regions (fig. 1).

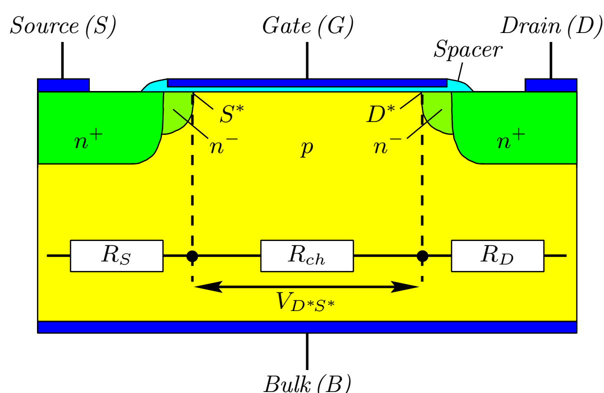

Figure 1: Source and drain resistances

In circuit simulators, e.g. Bsim3 v3.1, these resistances are either considered to be constant or modeled with a linear gate bias dependence [3]. Usually, the source and drain resistances are introduced with equal values ($R_S + R_D \approx 2 \cdot R_S$).

2. Simulation and Modeling

Medici simulations of a 0.25 μm technology N-MOSFET show a non-linear gate voltage behavior of the source resistance R_S (fig. 2).

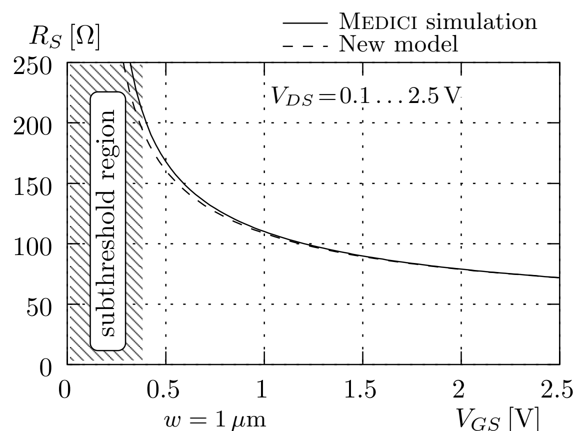

Figure 2: Comparison of Medici simulated source resistance with new model

Due to charge accumulation the resistance of the overlap region decreases with higher gate biases.
The source resistance is independent of the drain source bias and thus of the working region of the transistor. It can be modeled [1] by a resistance network the main part of which consists of a parallel connection of the resistance of the accumulation layer R_{acc} and the resistance R_{spr} which describes the spreading component (fig. 3).

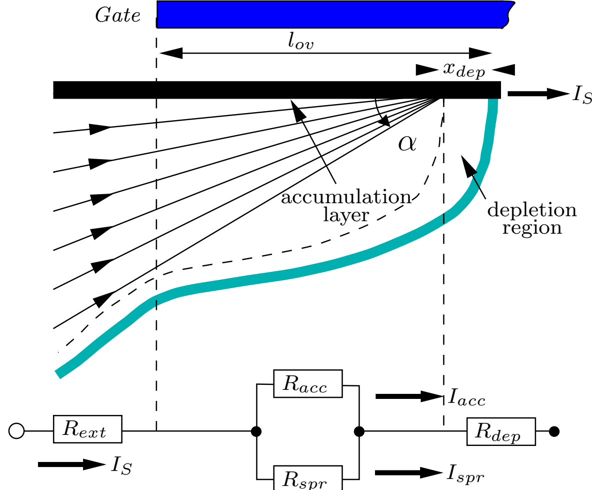

Figure 3: Model sceme

$$R_S = R_{ext} + \left(\frac{1}{R_{acc}} + \frac{1}{R_{spr}}\right)^{-1} + R_{dep}$$

with

$$\left(\frac{1}{R_{acc}(V_{GS})} + \frac{1}{R_{spr}}\right)^{-1} = \frac{1}{w\mu_n q\bar{N}_D \tan\alpha} \cdot \ln\left(1 + \frac{q\bar{N}_D \tan\alpha\,(l_{ov} - x_{depl})}{C'_{ox}\,(V_{GS} - V_{fb})}\right)$$

R_{ext} represents the constant extrinsic resistance and R_{dep} the resistance of the depletion region which can be modeled like an accumulation resistance:

$$R_{dep}(V_{GS}, V_{BS}) = \frac{x_{dep}}{w\mu_n C'_{ox}\,(V_{GS} - V_{fb})}$$

The width of the depletion region x_{dep} is substrat bias dependent:

$$x_{dep}(V_{BS}) = \sqrt{\frac{2\,\varepsilon_0\varepsilon_{si}}{q\bar{N}_D\left(1+\frac{\bar{N}_D}{N_A}\right)}\left(-V_{BS}+\phi_t \ln\frac{N_A\bar{N}_D}{n_i^2}\right)}$$

with an avarage doping concentration $\bar{N}_D$ over the overlap region and a spreading angle α. With the exact knowledge of R_S the inner gate source voltage (fig. 1)

$$V_{GS^*} = V_{GS} - R_S I_S$$

can be calculated which is important for the transconduction g_m of the transistor.

On the drain side one has to take into account that the effective gate bias is smaller than on the source side ($V_{GD} = V_{GS} - V_{DS}$) and thus causes less charge accumulation. Furthermore, the depletion region of the metallurgical junction is wider ($x_{dep} = f(V_{DB})$). As consequence the drain current starts spreading farther away from the junction.

Fig. 4 shows the simulated drain resistance which mainly differs from fig. 2 in a horizontal shift according to the magnitude of V_{DS}.

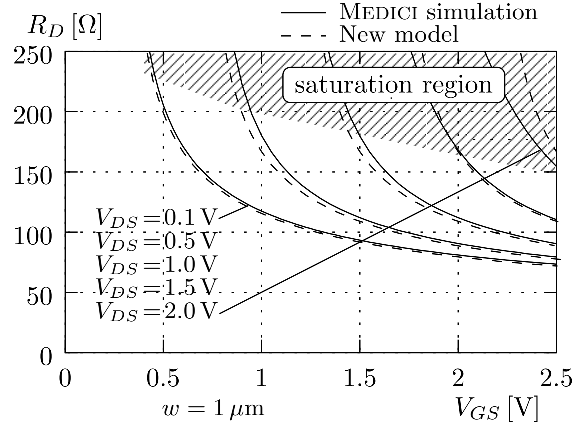

Figure 4: Comparison of MEDICI simulated drain resistance with new model for various drain source biases

With this description of R_S and R_D one is able to calculate the reduced drain source bias of the channel (fig. 1)

$$V_{D^*S^*} = V_{DS} - R_S I_S - R_D I_D$$

which is necessary to get a consistent AC/DC description of the transistor.

3. Implementation in Circuit Simulator and Measurements

To implement the model into a circuit simulator two possibilities are available:

i) introducing two interconnections and describe the source and drain resistors separately as shown in fig. 1 or

ii) reducing the increased calculation time by incorporating the resistors into the transistor equations as it is done by BSIM3 v3.1 [3].

Our proposed model was implemented in the popular BSIM3 v3.1 compact

model. BSIM3 v3.1 introduces the extrinsic source/drain resistance as a lumped resistance term R_{SD} by applying Ohm's law to the linear region current expression [4]:

$$I_{DS} = \frac{V_{DS}}{R_{tot}} = \frac{V_{DS}}{R_{ch} + R_{SD}}$$

$$\text{with} \quad R_{SD} = R_S + R_D$$

Originally, BSIM3 v3.1 does not differ between source and drain description and for that reason neglects varying drain source biases. Its modeling of R_{SD} is reduced to a linear V_{GS} dependence for the linear region of the transistor:

$$R_{SD} = C_1 + C_2 \cdot V_{GS} + f(V_{BS})$$
$$C_i = const \quad (i = 1, 2)$$

Fig. 5 shows a comparison of MEDICI simulated source/drain resistance in linear region with the new model and the original BSIM3 v3.1 description. To avoid discontinuity problems the resistance values are unchanged in the subthreshold and saturation region.

Obviously, BSIM3 v3.1 underestimates the resistance for low gate voltages as well as for high drain biases.

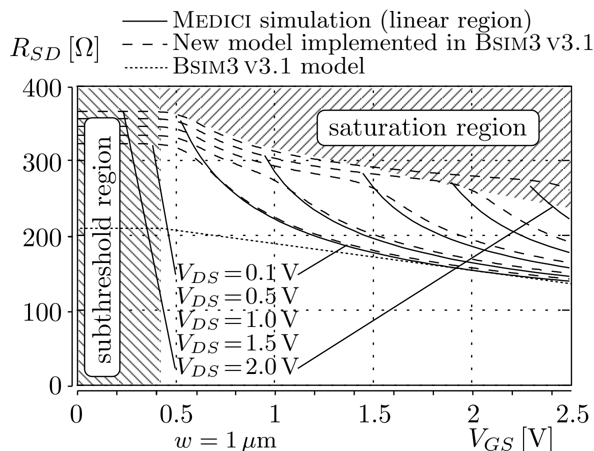

Figure 5: Comparison of MEDICI simulated source/drain resistance with new model and BSIM3 v3.1

To further verify our model, measurements on quarter micron technology MOSFETs [2] have been performed (fig. 6).

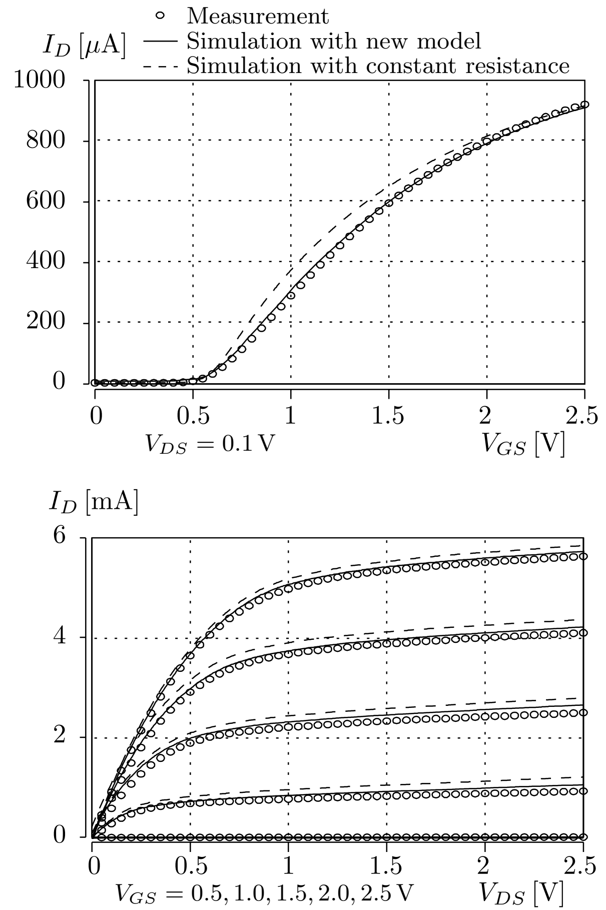

Figure 6: Measured and simulated characteristics ($w/l = 10\,\mu$m/$0.25\,\mu$m)

The comparison of simulation and measurement data demonstrates the influence of the introduced resistance model on the device characteristics.

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