Influence of the Inner Miller-Effect on the Input Capacitance of CMOS Transistors

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Abstract

The "inner Miller-effect" raises the input capacitance of MOS transistors in saturation from $^2/_3\,C_{ox}$ to C_{ox} for devices with shorter channel lengths. This paper analyses this behavior depending on the device length by measurements and device simulations. A model based on the capacitance $C_{ov,D}$ and the resistance $R_{ov,D}$ of the drain overlap region is presented.

1. Introduction

Helped by the continued down-scaling of device dimensions CMOS technologies conquer new markets (RF).
The input capacitance C_{in} is a key parameter in high-frequency circuit design. Therefore, there is a strong demand for compact models describing accurately also the small-signal behavior of MOSFETs.

Fig. 1 summarizes our proceeding in a flowchart.

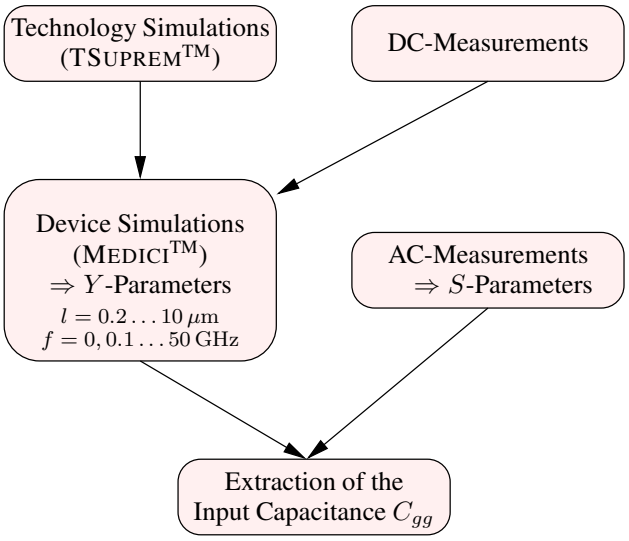


Figure 1: Proceeding of our investigations.

2. Device Simulations

The modeling of the input capacitance requires a well-defined separation of the inner transistor from parasitic effects [1].
Threfore we performed very accurate small-signal device simulations (MEDICI™). In order to reproduce our measured device performance, we executed technology simulations (TSUPREM™) on an industrial CMOS process as input for our device simulations.
Fig. 2 shows the relevant capacitances as a function of the gate-source voltage of a long and a short channel device ($V_{DS} = 1\,\mathrm{V}$).

We used the capacitance definitions from [2]:

$$C_{xy} = \frac{\partial Q_x}{\partial V_y} \quad \text{and} \tag{1}$$

$$C_{gg} + C_{sg} + C_{dg} + C_{bg} = 0 \tag{2}$$

For high gate voltages (triode region) the channel charge is distributed almost symmetrically along the channel. Thus, the source-gate capacitance C_{sg} and the drain-gate capacitance C_{dg} equal $^1/_2\,C_{ox}$. Diminishing the gate voltage under $V_{DS} + V_{th}$ turns the device into saturation, where the inversion charge decreases locally from source to drain.

For long-channel devices we could confirm the 60:40-partitioning of the inversion charge described in [3]. We expected the short channel partitioning to shift towards 50:50 due to channel length modulation as soon as we can consider the charge carriers to cross the channel with saturation velocity.
However, accurate device simulations reveal that for devices with gate lengths shorter than approx. $45\,\mathrm{nm}$ the drain capacitance exceeds the source capacitance and thus dominates the input capacitance (fig. 3).

Fig. 4 illustrates the increasing influence of the drain-gate capacitance by normalization on $C_{in} = C_{gg}$ and C_{ox}.

At $V_{DS} = V_{BS} = 0\,\mathrm{V}$ and $V_{GS} = -5\,\mathrm{V}$ the oxide capacitances (fig. 5) were extracted from the bulk-gate capaci-

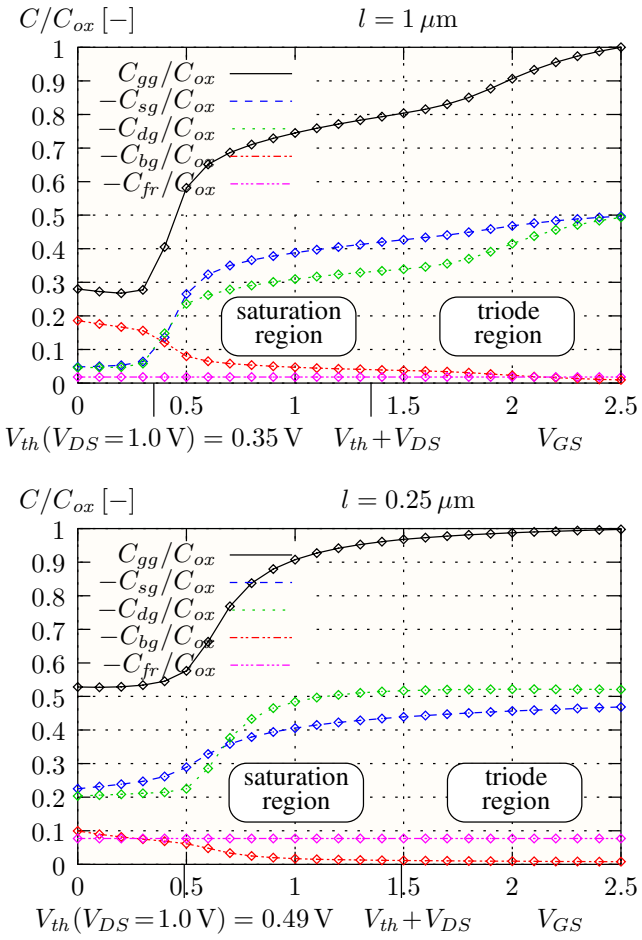


Figure 2: Capacitances vs. gate-source voltage for a long (1 μm) and a short (0.25 μm) device ($V_{DS} = 1$ V).

tances:

$$C_{ox} = C_{bg} \tag{3}$$

At the same bias conditions we obtained the fringing capacitances from:

$$C_{fr} = {}^1\!/_2\,(C_{sg} + C_{dg}) \tag{4}$$

The small variations of C_{bg} and C_{fr} can not explain the increasing input capacitance, as

$$|C_{bg} + C_{fr}| \approx \text{const} < 10\,\%\,C_{in}. \tag{5}$$

3. Measurements

We performed S-parameter measurements on CMOS finger structures ($w = 96\,\mu$m) in quarter micron technology. The small-signal scattering parameters (s_{xy}) have been corrected using a two-step de-embedding technique with open and short structures and were converted into y-parameters.

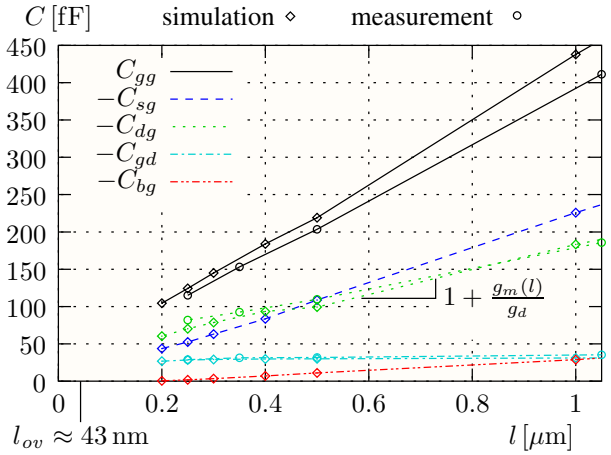


Figure 3: Capacitances vs. gate length ($V_{DS} = 2.5$ V, $V_{GS} = 1.0$ V, $w = 96\,\mu$m).

The extracted capacitances ($f = 100$ MHz)

$$C_{gg} = \text{Imag}\,(y_{11})\,/\,(2\,\pi f) \quad \text{and} \tag{6}$$
$$C_{dg} = \text{Imag}\,(y_{21})\,/\,(2\,\pi f) \tag{7}$$

of different devices show good agreement between our measurements and device simulations (figs. 3 and 4).

4. Model and Discussion

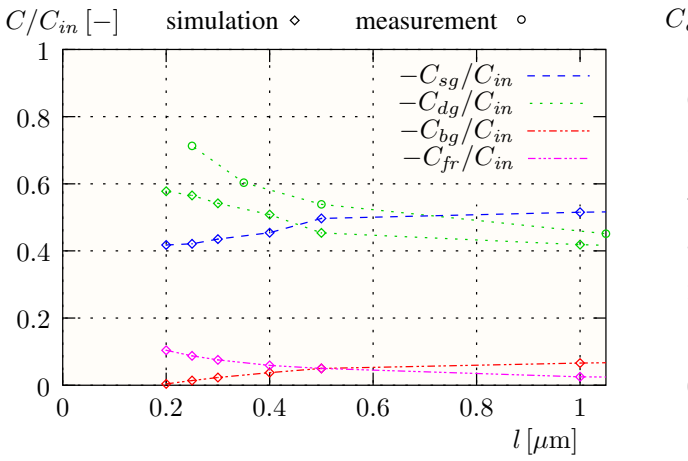
The increase of C_{in} can only be understood by dividing the device into its micro-circuit parts (fig. 6):
The gate couples to the drain over the channel and the overlap region.
The voltage $v_{ds\,sat}$ near the "pinchoff point" follows the gate-source voltage. Therefore, the capacitive contribution over the $R_{ch,D}$-$C_{ch,D}$ path can be neglected.
But the voltage v_{di} at the metallurgical junction of the drain decreases for increasing gate-source voltage because of the higher voltage drop over the parasitic drain resistance $R_D \approx R_{ov,D}$.

Therefore, the overlap capacitance $C_{ov,D}$ in combination with $R_{ov,D}$ has to be seen as an "inner Miller capacitance".

Fig. 7 shows the small-signal circuit equivalent to the above cross-section (fig. 6).

By solving the current-voltage equations of the above circuit the y-parameters can be achieved ($y_{gg} + y_{dg} + y_{sg} = 0$):

$$y_{21} = y_{dg} = \frac{g_d}{\left(\omega C^*_{dg}\right)^2 + g_d^2} \cdot \left[\left(\omega C^*_{dg}\right)^2 - g_m g_d + j\omega C^*_{dg}\,(g_d + g_m)\right] \tag{8}$$



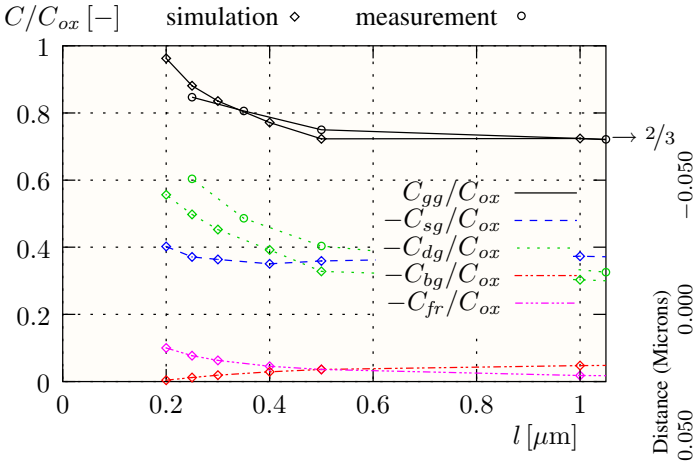


Figure 4: Normalized capacitances vs. gate length ($V_{DS} = 2.5\,\mathrm{V}, V_{GS} = 1.0\,\mathrm{V}, w = 96\,\mu\mathrm{m}$).

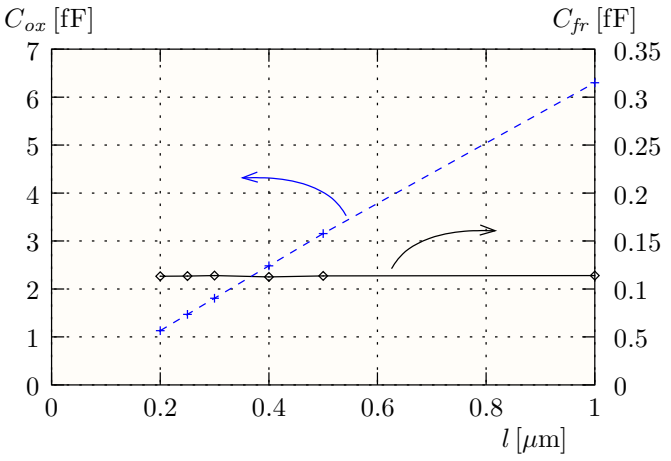


Figure 5: Extracted oxide and fringing capacitances.

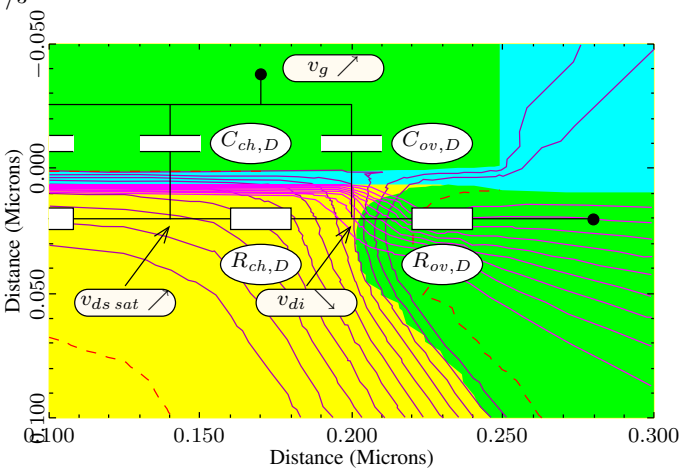


Figure 6: Overlap region of the drain with a distributed resistance-capacitance network.

$$
\begin{aligned}
y_{11} \;=\; y_{gg} &= \frac{-g_d}{\left(\omega C^*_{dg}\right)^2 + g_d^2} \cdot \\
&\cdot \left[\left(\omega C^*_{dg}\right)^2 - g_m g_d + j\omega C^*_{dg}\left(g_d + g_m\right)\right] + \\
&\frac{-g_s}{\left(\omega C^*_{sg}\right)^2 + g_s^2} \cdot \\
&\cdot \left[\left(\omega C^*_{sg}\right)^2 + g_m g_s + j\omega C^*_{sg}\left(g_s - g_m\right)\right] \\
&= -y_{21} - \frac{g_s}{\left(\omega C^*_{sg}\right)^2 + g_s^2} \cdot \\
&\cdot \left[\left(\omega C^*_{sg}\right)^2 + g_m g_s + j\omega C^*_{sg}\left(g_s - g_m\right)\right] \qquad (9)
\end{aligned}
$$

With $C^*_{dg} \approx C_{ov,D}$ and eq. (7) one obtains the amplified drain-gate capacitance.

$$
C_{dg} \;\approx\; C_{ov,D} \cdot \left(1 + \frac{g_m}{g_d}\right) \qquad (10)
$$

This model even explains the slight decrease of the source-gate capacitance C_{sg} in fig. 4 due to source degeneration ($v_g \nearrow\!\!\rightarrow v_{si} \nearrow$). (As the gate is low-resistive and in series to the parasitics, its contribution can be neglected.)

Similar to the well-known Miller-capacitance, the overlap capacitance $C_{ov,D}$ is amplified over its resistance $R_{ov,D}$.

As the overlap resistance has to be seen as a contributed resistance, it must be reduced to an effective value (in analogy to the describtion of e.g. the gate resistance).

$$
\begin{aligned}
1 + \frac{g_m}{g_d} \;&\approx\; 1 + {}^1\!/_3\, g_m R_D \approx 1 + {}^1\!/_3\, g_m R_{ov,D} \\
&\overset{\text{(fig. 8)}}{\approx}\; {}^1\!/_3\, g_m R_{ov,D} \qquad (11)
\end{aligned}
$$

For a given technology transistors of arbitrary gate lengths have equal overlap regions. Therefore, $R_{ov,D}$ and $C_{ov,D}$, which are functions of the overlap length l_{ov} and the dop-

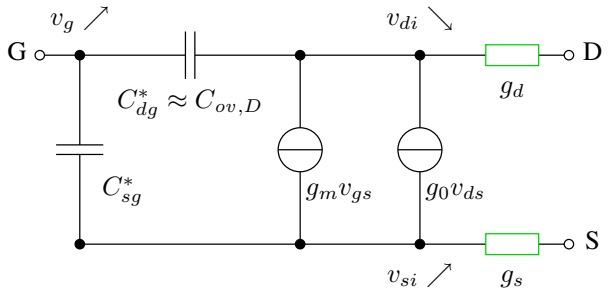


Figure 7: Small-signal circuit with parasitic resistances.

ing profile, only vary due to bias variation.

$$R_{ov,D} \neq R_{ov,D}(l) \quad \text{and} \quad C_{ov,D} \neq C_{ov,D}(l) \qquad (12)$$

The overlap region is inverted for negative V_{GD}. Whereas this slight decrease of $C_{ov,D}$ is well-understood [3], there is no concern taken about the dramatic increase of $R_{ov,D}$ (fig. 8).

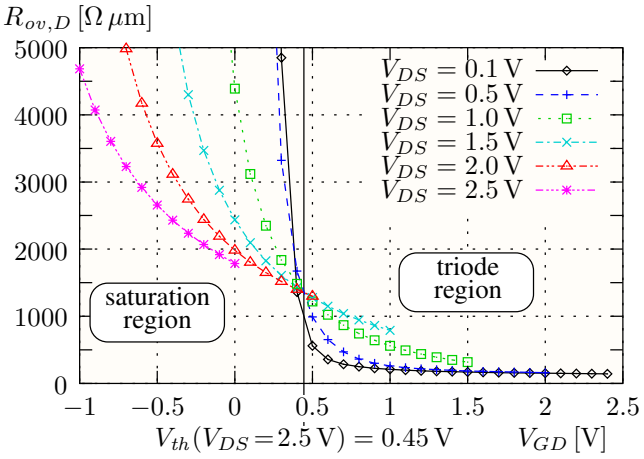


Figure 8: Drain overlap resistance vs. gate-drain voltage ($l = 0.25\,\mu$m).

Although this effect can be neglected for dc applications, as the channel resistance dominates in saturation, ac models have to focus on it.
Fig. 9 compairs the drain-gate capacitance extracted from measurements and MEDICI™ simulations with the Miller-gained overlap capacitance.

With the implementation of the overlap resistance [4]

$$R_D = \frac{1}{w\mu q N_{ov}\alpha} \cdot \ln\left(1 + \frac{qN_{ov}\alpha(l_{ov} - x_{dep})}{C_{ox}\,(V_{GD} - V_{FB_{ov}})}\right) \qquad (13)$$

in common CMOS models, the characteristics of the drain-gate capacitance can easily be adjusted to measurements.

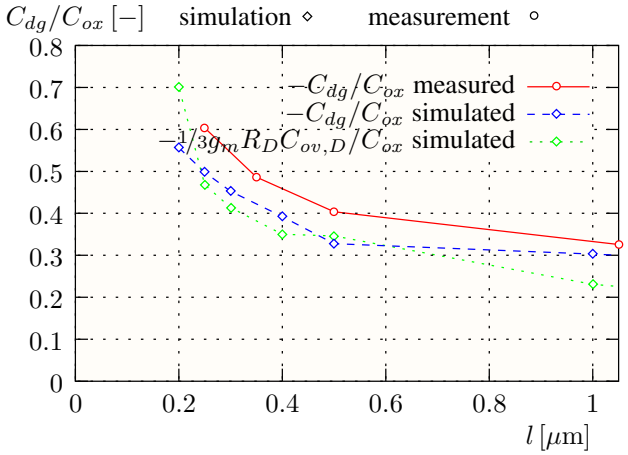


Figure 9: Normalized drain-gate capacitance and its proposed formulation vs. gate length from measurements and device simulation ($V_{DS} = 2.5$ V, $V_{GS} = 1.0$ V).

5. Conclusion

Since the drain-gate capacitance contributes to the input capacitance

$$\begin{aligned} C_{in} &= C_{gg} = C_{dg} + C_{sg}(+C_{bg}) \qquad (14) \\ &= C_{ov,D} \cdot (1 + {}^1\!/_3\, g_m R_D) + C_{sg}(+C_{bg}), \end{aligned}$$

the "inner Miller-effect" causes C_{in} to increase far above ${}^2\!/_3\, C_{ox}$. By extrapolation we expect C_{in} to be even bigger than C_{ox} for gate lengths shorter than approx. $0.17\,\mu$m.

As consequence, the desired input performance must be increased and the transit frequency is over-estimated.

Common four-nodes-models can not describe this "inner Miller-effect", because it can only be understood through the $R_{ov,D}C_{ov,D}$-network.

[1] E. Gondro, F. Schuler, and P. Klein. *A Physics Based Resistance Model of the Overlap Regions in LDD-MOSFETs*. In K. De Meyer and S. Biesemans, editors, *Simulation of Semiconductor Processes and Devices (SISPAD'98)*, pages 267–270, Leuven, Belgium, September 1998. Springer-Verlag Wien NewYork.

[2] Y. Tsividis. *Operation and Modeling of the MOS Transistor*. Electronics and Electronic Circuits. WCB McGraw-Hill, NewYork, 2. edition, 1999.

[3] W. Liu, X. Jin, K. M. Cao, and C. Hu. *BSIM4.0.0 MOSFET Model — User's Manual*. Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, California 94720, USA, 2000.

[4] E. Gondro, P. Klein, and F. Schuler. *An Analytical Source-and-Drain Series Resistance Model of Quarter Micron MOSFETs and its Influence on Circuit Simulation*. In *IEEE International Symposium on Circuits and Systems (ISCAS'99)*, volume 6, pages 206–209, Orlando, Florida, USA, May 1999.